REMARKS

Claims 1-37 remain pending in the present application. In the Office Action, claims 1-9, 11-19, 21, 23-25, 27-34, and 36-37 were rejected under 35 U.S.C. § 102(b) as allegedly being anticipated by Maruyama (U.S. Patent No. 6,052,763). The Examiner's rejections are respectfully traversed.

Maruyama is directed to a memory unit and a method for coordinating atomic memory transactions in a tightly coupled multiprocessor system. Maruyama describes a system bus 15 and a system bus interface 16 coupled to a decoder 21, a register 22, a comparator 23, and a master ID table 24. See Maruyama, Figure 4. The system bus 15 and the system bus interface 16 provide an access address to the decoder 21, which identifies whether the access address is for a conventional address space or for an atomic address space. See Maruyama, col. 6, ll. 11-15. The system bus 15 and the system bus interface 16 also provide a bus master ID to the register 22, the comparator 23, and the master ID table 24. See Maruyama, col. 6, ll. 44-47. In an atomic transaction mode, an ID of the bus master that is making the atomic transaction request is temporally stored in the register 22. Subsequently, the comparator 23 compares the temporally stored bus master ID with the ID of the requesting device. See Maruyama, col. 7, ll. 26-34. The master ID table 24 uses the bus master ID to distinguish whether or not a bus master is a processor. See Maruyama, col. 6, ll. 47-50.

The Examiner alleges that the comparator 23 compares values from the master ID table 24 to the bus master ID. Applicants respectfully disagree. As stated above, the comparator 23 does not access the bus master ID table 24 and instead compares the bus master ID that is temporally stored in register 22 with the ID of the requesting device that is provided by the system bus interface 16. Moreover, as also stated above, the bus master ID table 24 uses the bus

master ID (provided by the system bus interface 16) to distinguish whether or not a bus master is a processor. Thus, Applicants respectfully submit that Maruyama fails to teach or suggest a security check unit configured to use the physical address to access at least one security attribute data structure located in the memory to obtain a security attribute of the selected memory page, as set forth in independent claims 1, 11-13, 23, and 32. Consequently, Maruyama also fails to teach or suggest comparing information, such as a numerical value, conveyed by a security attribute of the current instruction to information, such as a numerical value, conveyed by the security attribute of the selected memory page, producing an output signal dependent upon a result of the comparison, or accessing the selected memory page dependent upon the output signal.

For at least the aforementioned reasons, Applicants respectfully submit that independent claims 1, 11-13, 23, 32, and all claims depending therefrom are not anticipated by Maruyama and request that the Examiner's rejections of these claims under 35 U.S.C. 102(b) be withdrawn.

In the Office Action, claims 10, 20, 22, 26, and 35 were rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over Maruyama in view of Applicants' admitted prior art. The Examiner's rejections are respectfully traversed.

To establish a *prima facie* case of obviousness, the prior art reference (or references when combined) must teach or suggest all the claim limitations. *In re Royka*, 490 F.2d 981, 180 U.S.P.Q. 580 (CCPA 1974). Claims 10, 20, 22, 26, and 35 depend from independent claims 1, 13, 23, and 32. As discussed above, Maruyama fails to teach or suggest many aspects of the present invention set forth in independent claims 1, 13, 23, and 32. The Examiner relies on the admitted prior art to teach use of a user/supervisor bit and/or a read/write bit. However, Applicants respectfully submit that the admitted prior art does not remedy the fundamental

PAGE 19/20 * RCVD AT 3/16/2004 4:36:19 PM [Eastern Standard Time] * SVR:USPTO-EFXRF-1/4 * DNIS:8729306 * CSID:7139347011 * DURATION (mm-ss):05-22

deficiencies of the primary reference. Thus, Applicants respectfully submit that claims 10, 20, 22, 26, and 35 are not obvious over Maruyama in view of the admitted prior art and request that the Examiner's rejections of these claims under 35 U.S.C. 103(a) be withdrawn.

In the Office Action, the Examiner provisionally rejected claims 1-37 under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-37 of co-pending Application Number 10/010,161. In the interest of expediency, Applicant has included herein a terminal disclaimer and respectfully requests that the Examiner's rejection of claims 1-37 be withdrawn. However, it will be appreciated that the filing of the terminal disclaimer to obviate the Examiner's rejection is not an admission of the propriety of the rejection. *Quad Environmental Technologies Corp. vs. Union Sanitary District*, 946 F.2d 870, 20 USPQ2d 1392 (Fed Cir. 1991). See, *e.g.*, MPEP §804.03.

For the aforementioned reasons, it is respectfully submitted that all claims pending in the present application are in condition for allowance. The Examiner is invited to contact the undersigned at (713) 934-4052 with any questions, comments or suggestions relating to the referenced patent application.

Respectfully submitted,

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PAGE 20/20 * RCVD AT 3/16/2004 4:36:19 PM [Eastern Standard Time] * SVR:USPTO-EFXRF-1/4 * DNIS:8729306 * CSID:7139347011 * DURATION (mm-ss):05-22